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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,561	08/19/2003	Hsueh-Yuan Pao	IL-11028	6617
7590	09/12/2005		EXAMINER	
Deputy Laboratory Counsel For Intellectual Property Lawrence Livermore National Laboratory P.O. Box 808, L-703 Livermore, CA 94551			FILE, ERIN M	
			ART UNIT	PAPER NUMBER
			2634	
			DATE MAILED: 09/12/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
10/644,561	PAO ET AL.
Examiner	Art Unit
Erin M. File	2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 06 June 2005.
2a) This action is FINAL. 2b) This action is non-final.
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-12 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) Claim(s) _____ is/are allowed.
6) Claim(s) 1-12 is/are rejected.
7) Claim(s) _____ is/are objected to.
8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
10) The drawing(s) filed on 06 June 2005 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
5) Notice of Informal Patent Application (PTO-152)
6) Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1 -12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang and in further view of Becker.

Claim 1, 7, 12, Zhang discloses a serial-to-parallel data converter which converts a string of serial data to a plurality of parallel data (fig. 1, 21); in-phase/quadrature mapper that receives parallel data and determines its I and Q locations (fig. 2, 47, col. 5, lines 21-40); a plurality of look-up-tables (LUTs) operatively connected to receive and store said I and Q locations, wherein the in-phase LUTs are configured I_1 to I_N , and quadrature LUTs are configured Q_1 to Q_X (abstract, fig. 6B, col. 5, lines 21-40); a adders to receive and add I and Q locations stored within LUTs, wherein adders are configured A_1 to A_{AN} , wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN} (fig. 6B); registers to collect and store IQ_1 to IQ_{IQN} (col. 5, lines 10-46); a digital to analog

converter operatively connected to convert said output data comprising IQ_1 to IQ_{IQ_N} to analog data (fig. 2, 53). Zhang fails to disclose a quadrature amplitude modulator which does not include a multiplier, Becker discloses an architecture for a universal modulator which can function in a variety of modes including QAM without the use of multipliers (abstract). Zhang teaches a quadrature amplitude modulator which meets all of the limitations of the disclosed invention, and further teaches his invention significantly reduces the number of multipliers (abstract). Becker teaches a modulator which can function in a variety of modes including quadrature amplitude modulation and does not disclose the use of any modulators. Because of Zhang's disclosure teaches away from the use of multipliers in his modulation technique, claiming an increase in the efficiency of the modulation, it would be obvious to one skilled in the art at the time of invention to incorporate Becker's modulation technique into Zhang's invention.

Claims 2, 8, 10, Zhang discloses a serial-to-parallel data converter which converts a string of serial data to a plurality of parallel data (fig. 1, 21); in-phase/quadrature mapper that receives parallel data and determines its I and Q locations (fig. 2, 47, col. 5, lines 21-40); a plurality of look-up-tables (LUTs) operatively connected to receive and store said I and Q locations, wherein the in-phase LUTs are configured I_1 to I_N , and quadrature LUTs are configured Q_1 to Q_x (abstract, fig. 6B, col. 5, lines 21-40); a adders to receive and add I and Q locations stored within LUTs, wherein adders are configured A_1 to A_{AN} , wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQ_N} (fig.

6B); registers to collect and store IQ_1 to IQ_{IQ_N} (col. 5, lines 10-46); at least one multiplexer to collect from registers the subscript output data comprising only odd subscript output data from said output data comprising IQ_1 to IQ_{IQ_N} (fig. 3B); at least one multiplexer to collect from said plurality of registers the subscript output data comprising only even subscript output data from said output data comprising IQ_1 to IQ_{IQ_N} (fig. 3A); and a digital to analog converter operatively connected to convert said odd subscript data and said even subscript data to analog data (fig. 2, 53). Zhang fails to disclose a quadrature amplitude modulator which does not include a multiplier, Becker discloses an architecture for a universal modulator which can function in a variety of modes including QAM without the use of multipliers (abstract). Zhang teaches a quadrature amplitude modulator which meets all of the limitations of the disclosed invention, and further teaches his invention significantly reduces the number of multipliers (abstract). Becker teaches a modulator which can function in a variety of modes including quadrature amplitude modulation and does not disclose the use of any modulators. Because of Zhang's disclosure teaches away from the use of multipliers in his modulation technique, claiming an increase in the efficiency of the modulation, it would be obvious to one skilled in the art at the time of invention to incorporate Becker's modulation technique into Zhang's invention.

Claims 3, 5, 9, 11, Zhang meets all the limitations of claims 3, 5, 9, and 11, (see above paragraphs) except disclosing the exact multiplexer configuration wherein $nx2$

multiplexers are used. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use various permutations of multiplexers since it is well-known in the art that there are multiple ways to translate multiple signals into one output. For instance, Zhang could use two 4x2 and two 2x1 multiplexers to substitute for one 8x1 multiplexer. In addition, applicant has not disclosed that nx2 multiplexers provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with one 8x1 multiplexer because it would reduce FPGA programming complexity. Therefore, it would have been obvious to one of ordinary skill in this art to modify Zhang to obtain the invention as specified in claims 3, 5, 9, and 11.

Claim 4, Zhang discloses a plurality of look-up-tables (LUTs) operatively connected to receive and store said I and Q locations, wherein the in-phase LUTs are configured I₁ to I_N, and quadrature LUTs are configured Q₁ to Q_X (abstract, fig. 6B, col. 5, lines 21-40); a adders to receive and add I and Q locations stored within LUTs, wherein adders are configured A₁ to A_{AN}, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ₁ to IQ_{IQN} (fig. 6B); registers to collect and store IQ₁ to IQ_{IQN} (col. 5, lines 10-46); at least one multiplexer to collect from registers the subscript output data comprising only odd subscript output data from said output data comprising IQ₁ to IQ_{IQN} (fig. 3B); at least one multiplexer to collect from said plurality of registers the subscript output data comprising only even subscript output data from said output data comprising IQ₁ to IQ_{IQN} (fig. 3A);

and a digital to analog converter operatively connected to convert said odd subscript data and said even subscript data to analog data (fig. 2, 53). Zhang fails to disclose a quadrature amplitude modulator which does not include a multiplier, Becker discloses an architecture for a universal modulator which can function in a variety of modes including QAM without the use of multipliers (abstract). Zhang teaches a quadrature amplitude modulator which meets all of the limitations of the disclosed invention, and further teaches his invention significantly reduces the number of multipliers (abstract). Becker teaches a modulator which can function in a variety of modes including quadrature amplitude modulation and does not disclose the use of any modulators. Because of Zhang's disclosure teaches away from the use of multipliers in his modulation technique, claiming an increase in the efficiency of the modulation, it would be obvious to one skilled in the art at the time of invention to incorporate Becker's modulation technique into Zhang's invention.

Claim 6, Zhang discloses a plurality of look-up-tables (LUTs) operatively connected to receive and store said I and Q locations, wherein the in-phase LUTs are configured I₁ to I_N, and quadrature LUTs are configured Q₁ to Q_X (abstract, fig. 6B, col. 5, lines 21-40); a adders to receive and add I and Q locations stored within LUTs, wherein adders are configured A₁ to A_{AN}, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ₁ to IQ_{IQN} (fig. 6B); registers to collect and store IQ₁ to IQ_{IQN} (col. 5, lines 10-46); a digital to analog converter operatively connected to convert said odd subscript data and said even

subscript data to analog data (fig. 2, 53). Zhang fails to disclose a quadrature amplitude modulator which does not include a multiplier, Becker discloses an architecture for a universal modulator which can function in a variety of modes including QAM without the use of multipliers (abstract). Zhang teaches a quadrature amplitude modulator which meets all of the limitations of the disclosed invention, and further teaches his invention significantly reduces the number of multipliers (abstract). Becker teaches a modulator which can function in a variety of modes including quadrature amplitude modulation and does not disclose the use of any modulators. Because of Zhang's disclosure teaches away from the use of multipliers in his modulation technique, claiming an increase in the efficiency of the modulation, it would be obvious to one skilled in the art at the time of invention to incorporate Becker's modulation technique into Zhang's invention.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erin M. File whose telephone number is (571)272-6040. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571)272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Erin M. File

EF

8/29/2005


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